FIG. 1

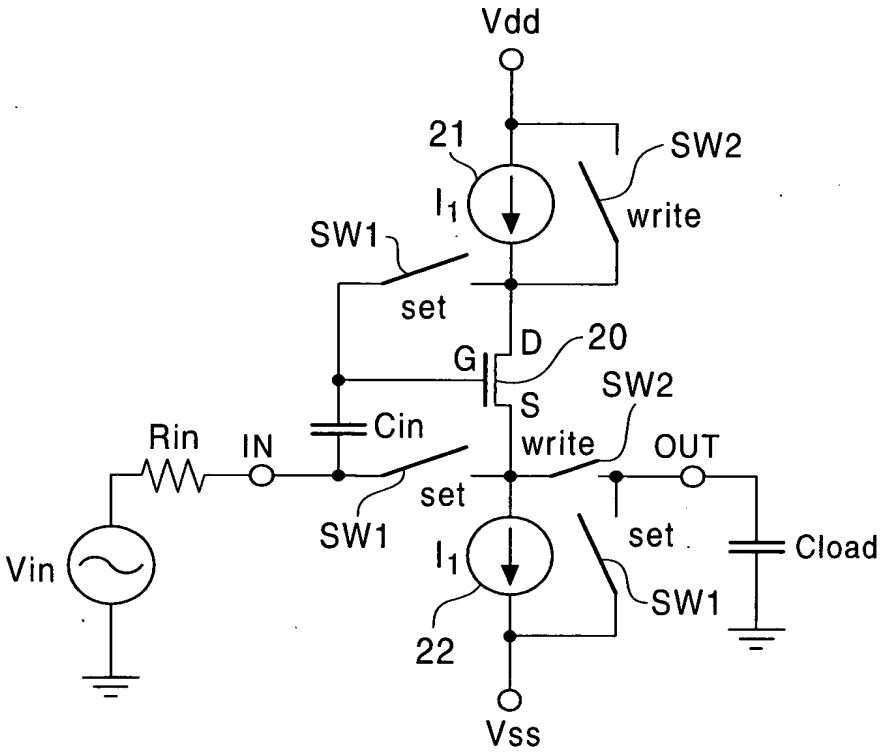

Vdd
21
SW2
I_1
write
SW1
set
G
D
20
S
SW2
Rin
IN
Cin
write
OUT
set
set
Cload
Vin
SW1
I_1
SW1
22
Vss

FIG. 2

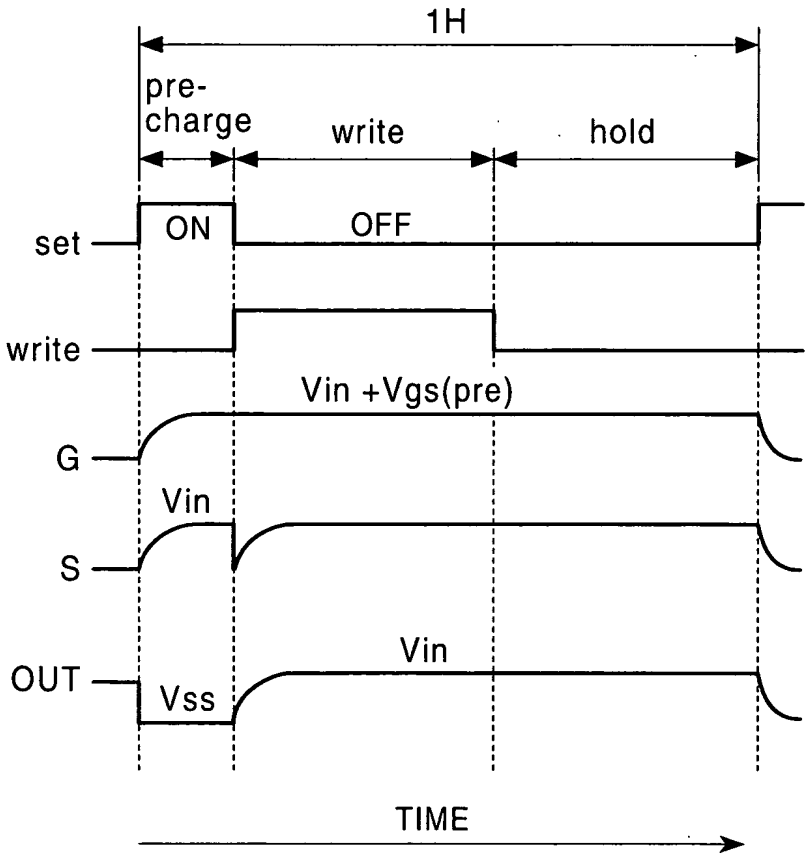

1H
pre-
charge
write
hold
set
ON
OFF
write
Vin +Vgs(pre)
G
Vin
S
Vin
OUT
Vss
TIME

FIG. 3

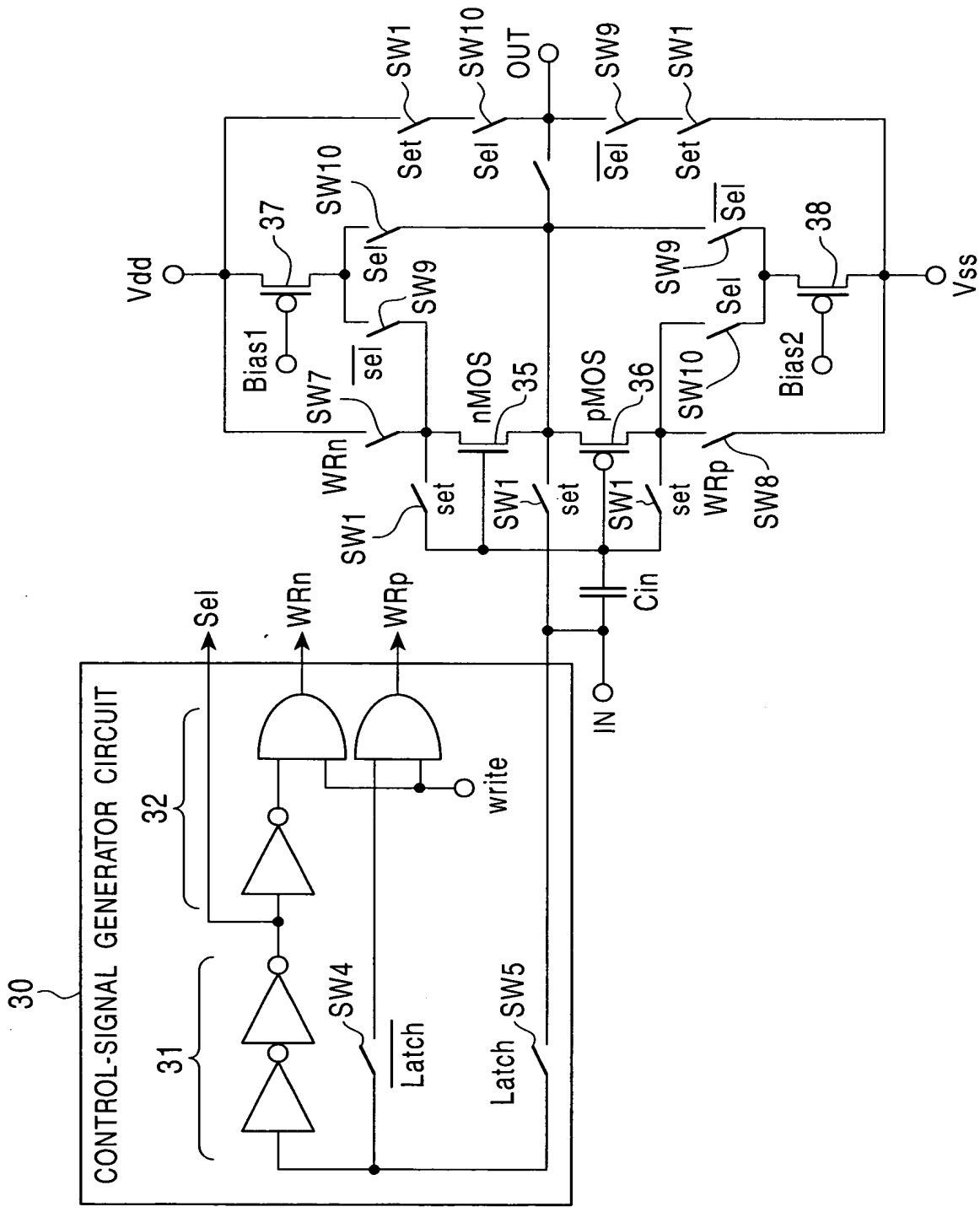

CONTROL-SIGNAL GENERATOR CIRCUIT
30
31
32
Sel
WRn
WRp
write
SW4
SW5
Latch
Latch
IN
Cin
SW1
SW10
OUT
SW9
SW1
Set
Sel
Sel
Set
37
38
Vdd
Vss
Bias1
Bias2
SW7
SW10
SW9
SW9
SW10
sel
Sel
Sel
nMOS
35
pMOS
36
WRn
WRp
SW8
SW1
set
SW1
set
SW1
set

FIG. 4

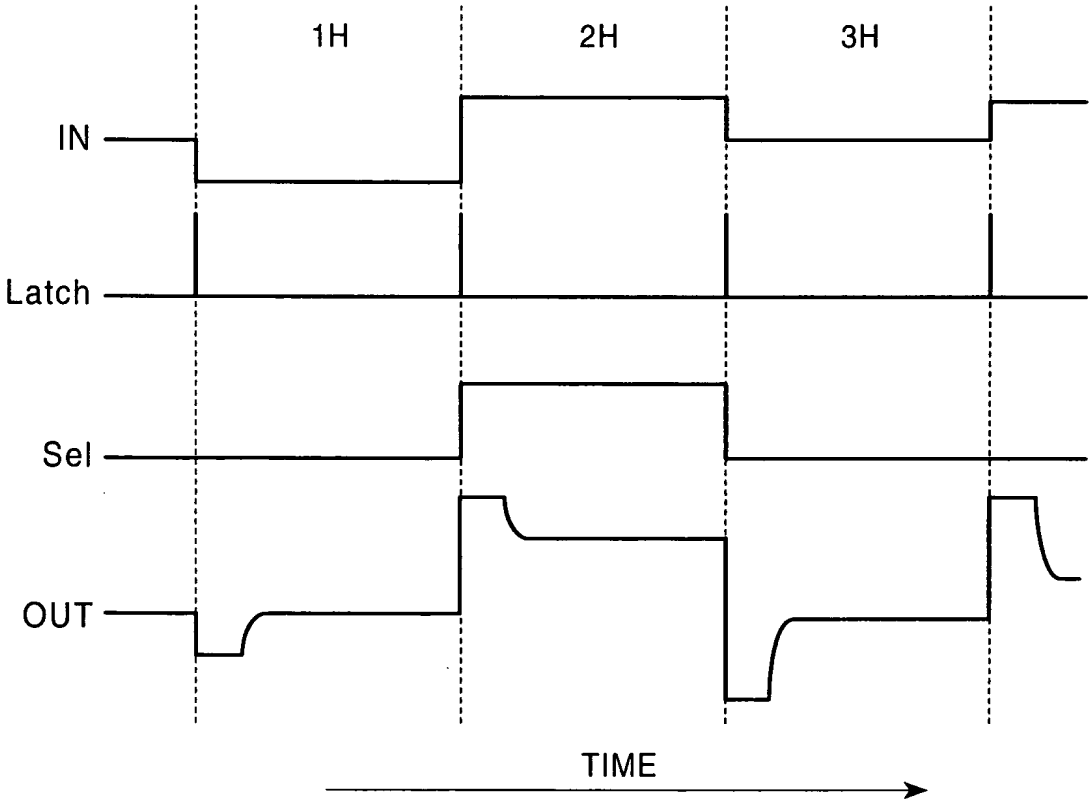


FIG. 5

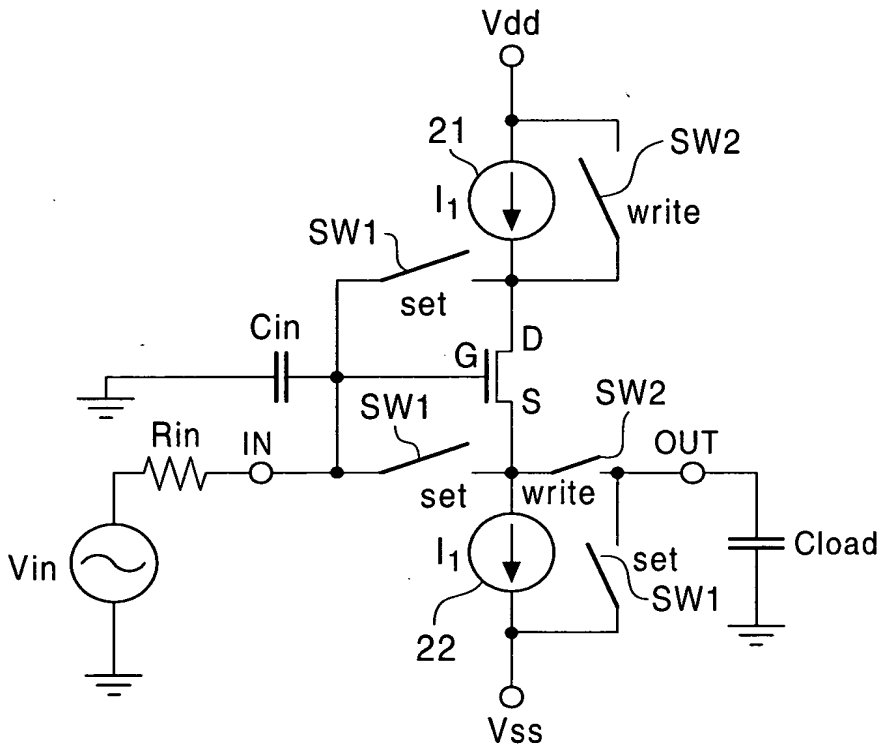

Vdd
21
SW2
I_1
write
SW1
set
Cin
D
G
S
SW1
SW2
Rin
IN
OUT
set
write
Vin
I_1
set
SW1
Cload
22
Vss

FIG. 6

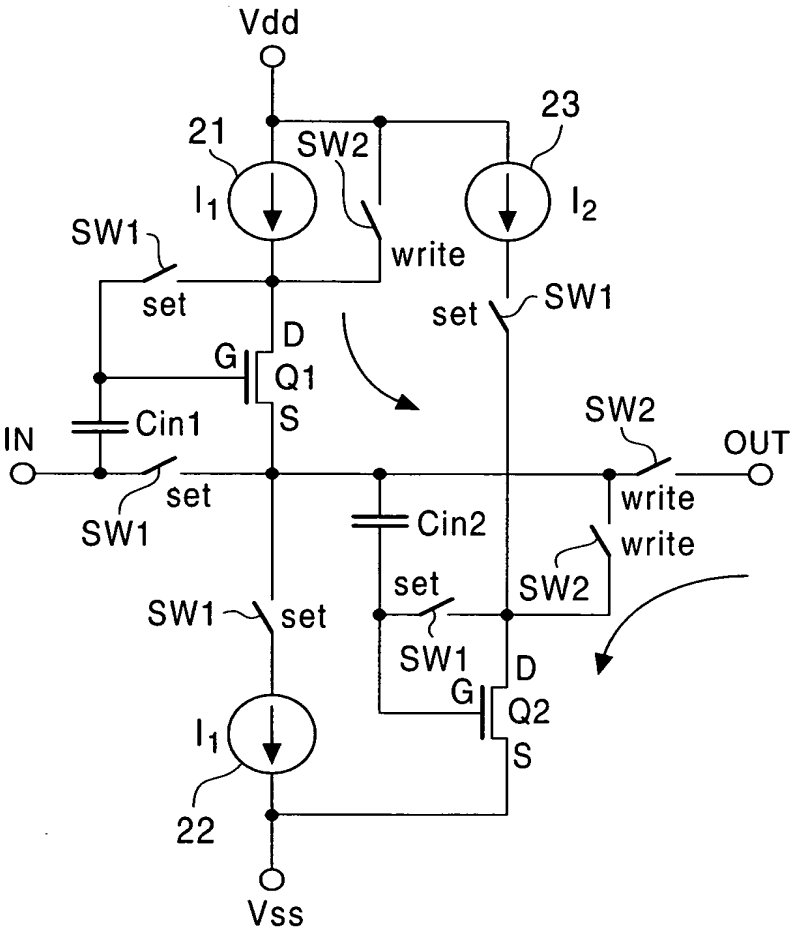

Vdd
21
SW2
23
I_1
I_2
SW1
write
set
set
SW1
D
G
Q1
S
IN
Cin1
SW2
OUT
set
write
SW1
Cin2
write
set
SW2
SW1
set
SW1
D
G
Q2
S
I_1
22
Vss

FIG. 7

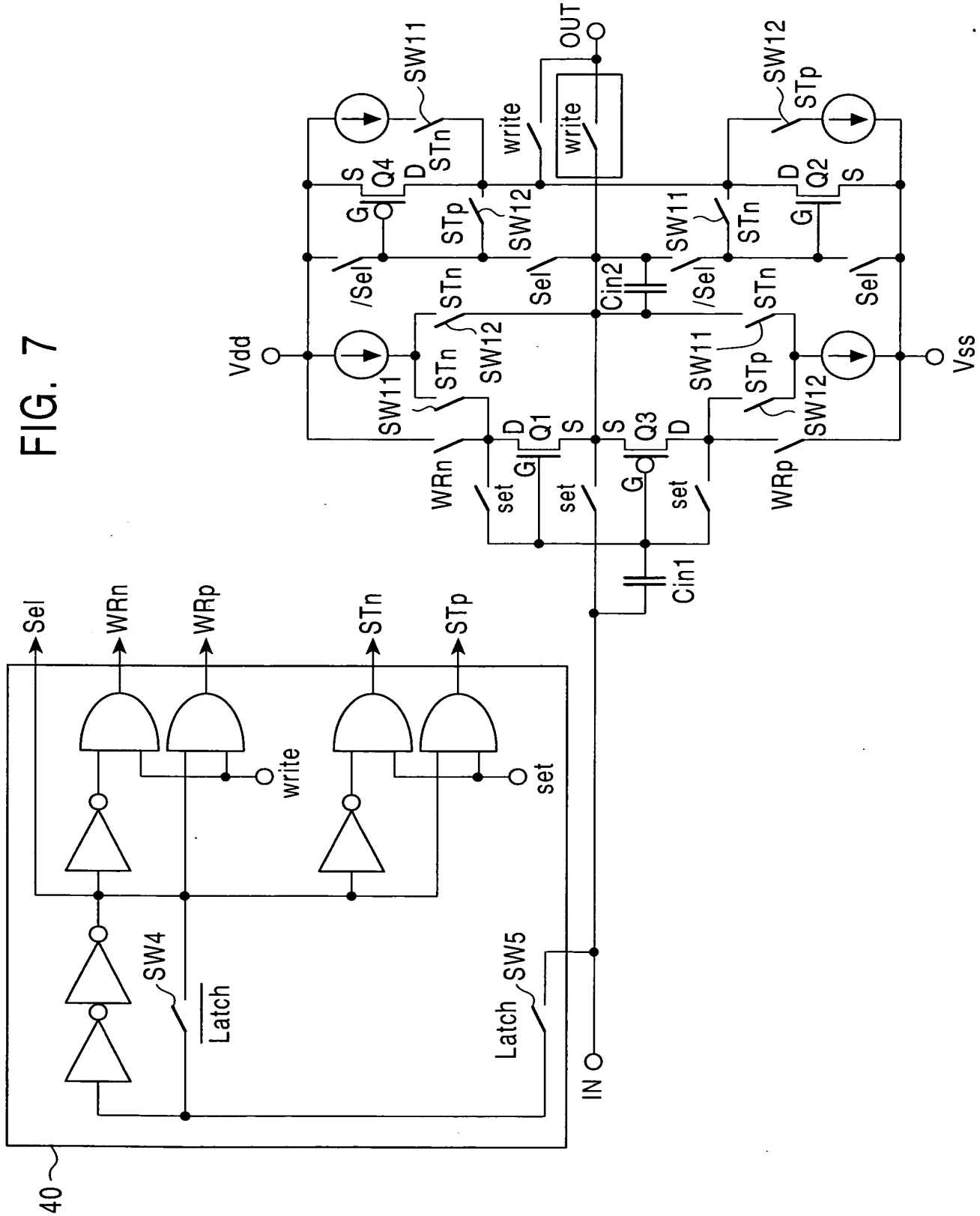

Vdd
Vss
OUT
IN
Sel
WRn
WRp
STn
STp
write
set
Latch
SW4
SW5
SW11
SW12
Cin1
Cin2
Q1
Q2
Q3
Q4
40

FIG. 8A

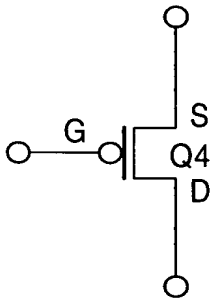


FIG. 8B

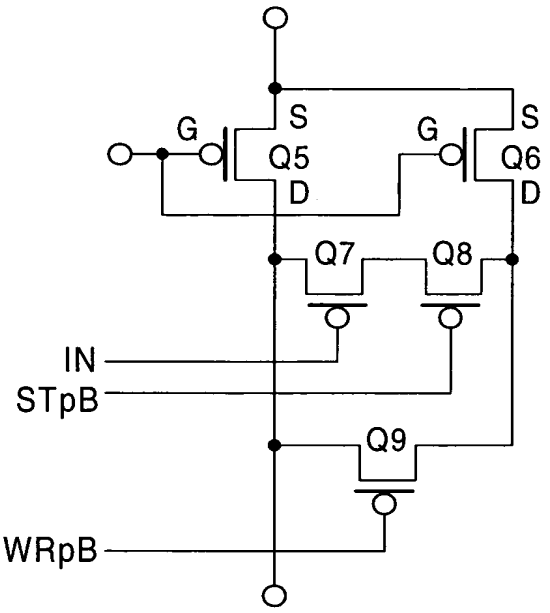


FIG. 9

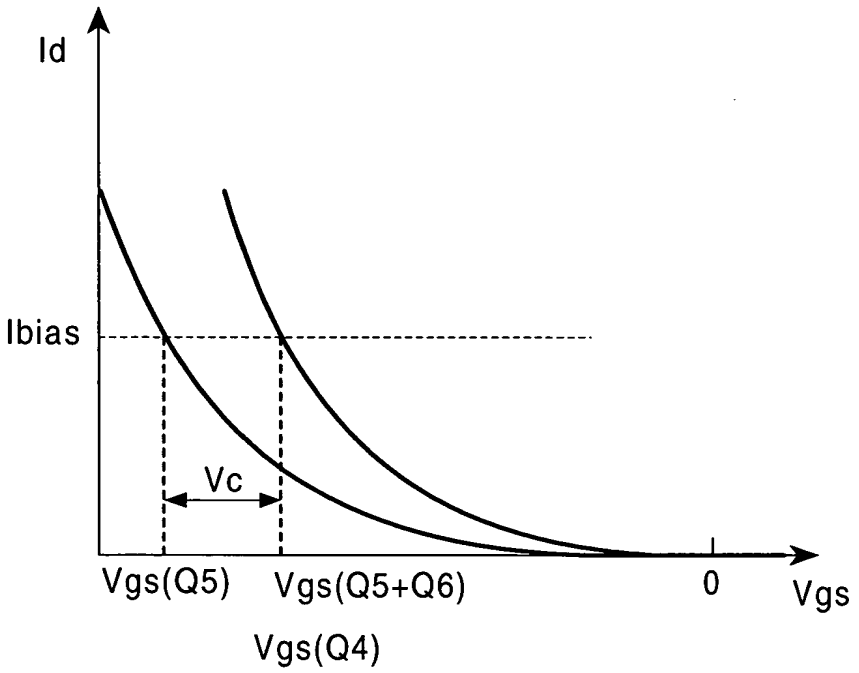


FIG. 10

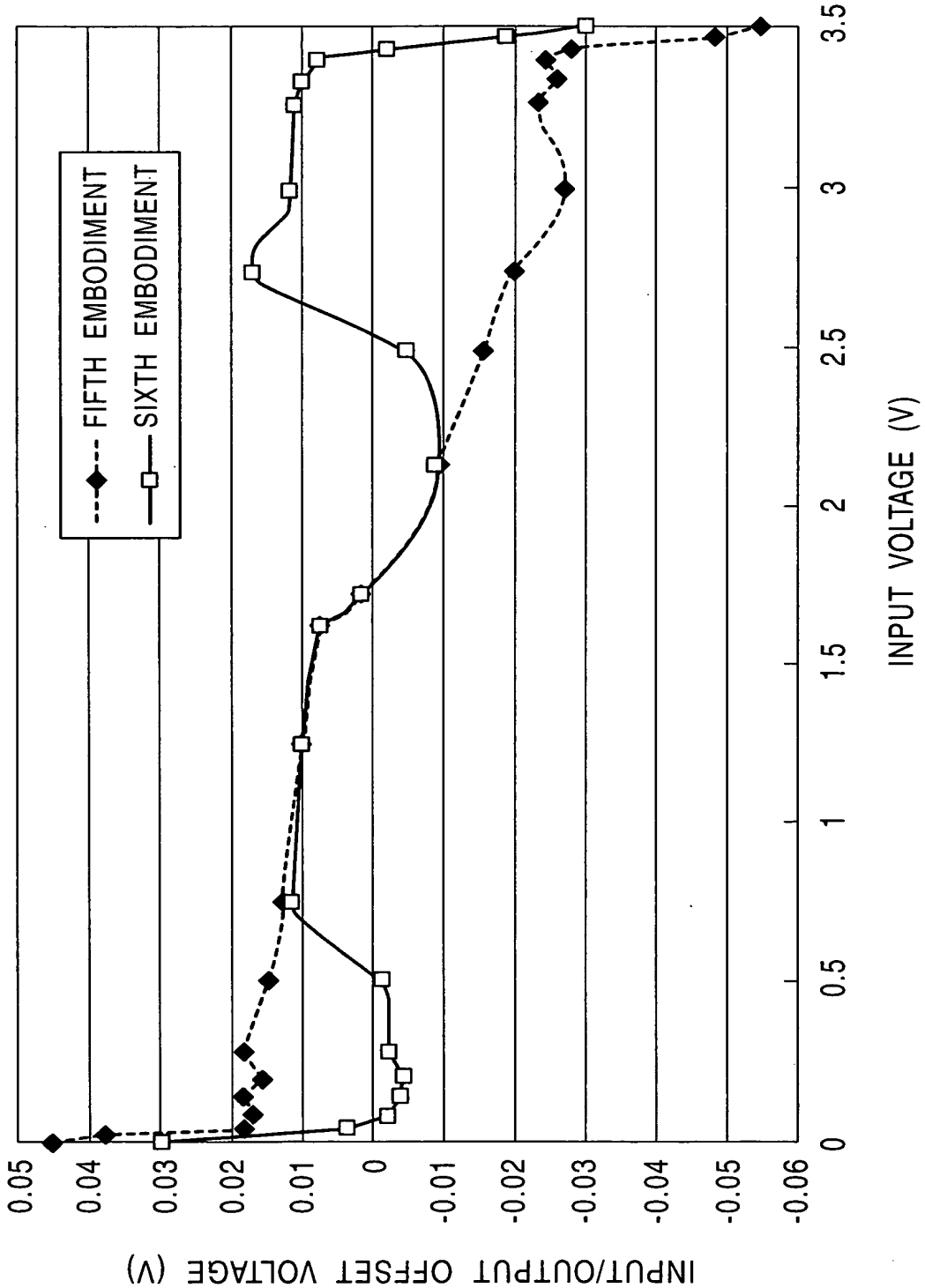
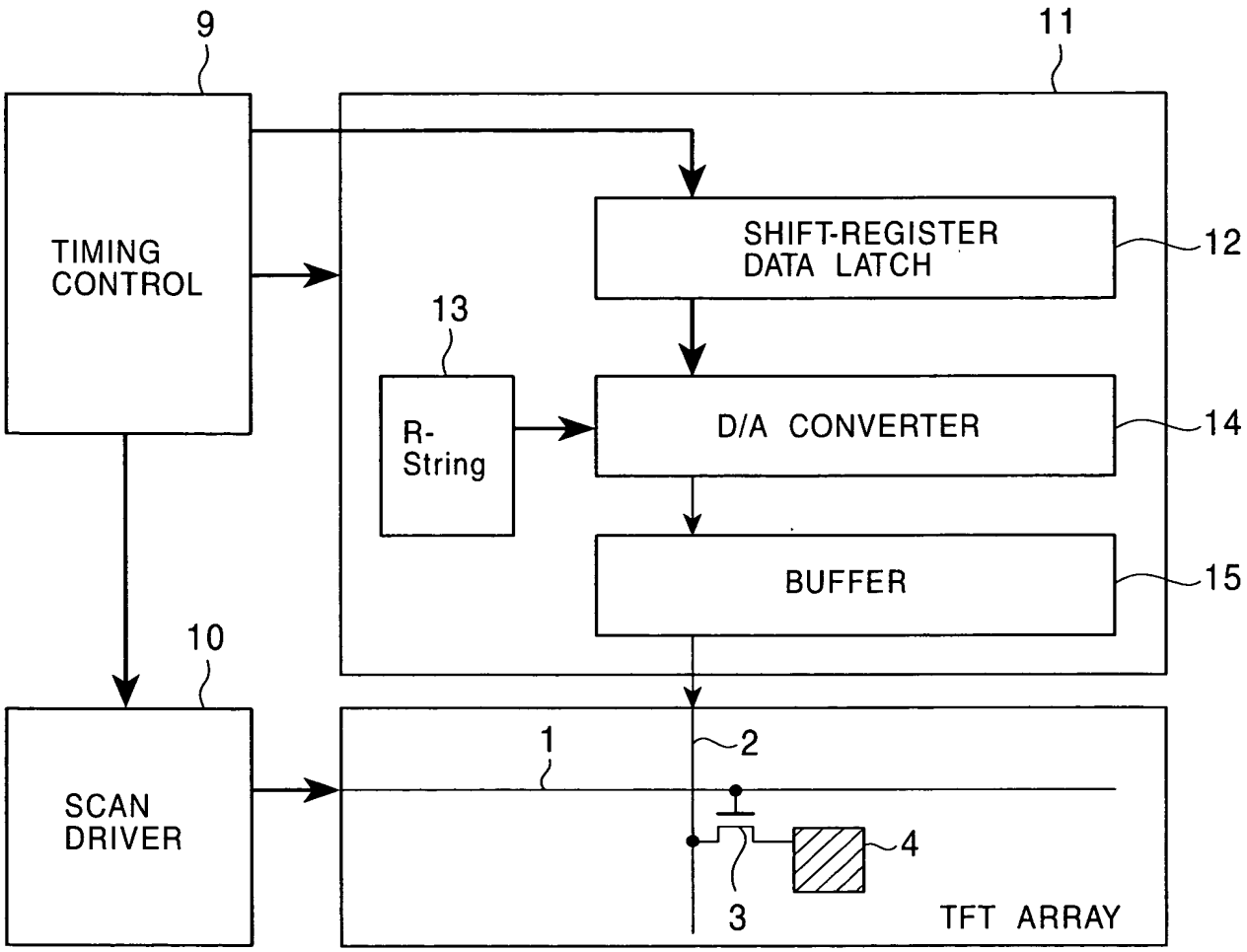

FIFTH EMBODIMENT
SIXTH EMBODIMENT
INPUT/OUTPUT OFFSET VOLTAGE (V)
INPUT VOLTAGE (V)
0.05
0.04
0.03
0.02
0.01
0
-0.01
-0.02
-0.03
-0.04
-0.05
-0.06
0
0.5
1
1.5
2
2.5
3
3.5

FIG. 11


9
11
TIMING CONTROL
SHIFT-REGISTER DATA LATCH
12
13
R-String
D/A CONVERTER
14
BUFFER
15
10
SCAN DRIVER
1
2
4
3
TFT ARRAY

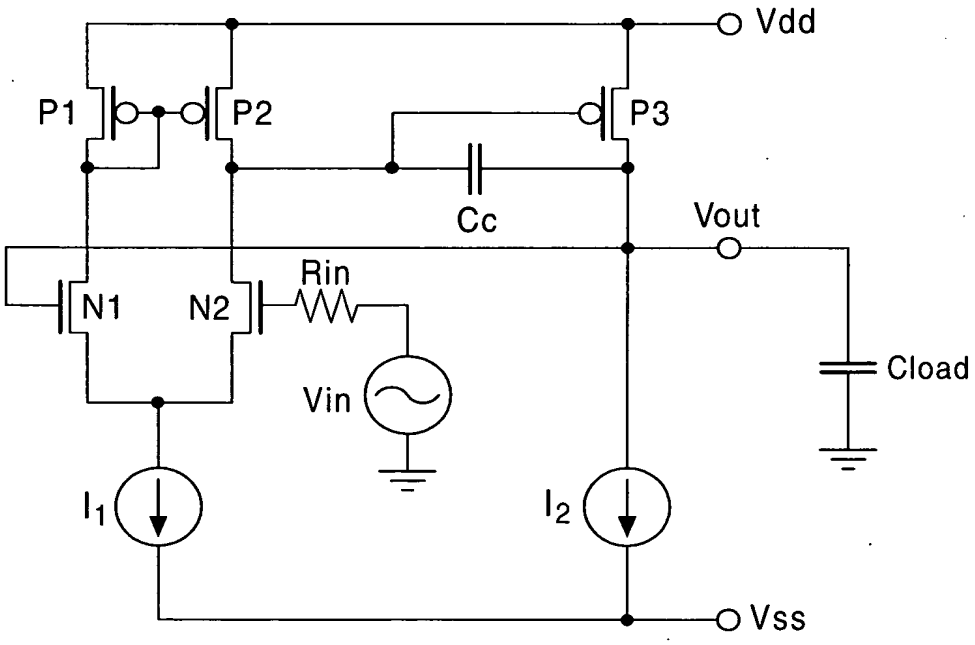



FIG. 12